1. A memory module, comprising:

a. a memory cell having a memory state; and

b. a local sense amplifier coupled with the memory cell, the local sense amplifier sensing the memory state and producing a local memory state signal representative thereof, wherein the local sense amplifier produces a limited swing voltage signal.

2. The memory module of Claim 1, further comprising a global sense amplifier, coupled with the local sense amplifier, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof.

3. The memory module of Claim 1, further comprising a plurality of memory cells coupled with the local sense amplifier.

4. The memory module of claim 3, further comprising:

a. a plurality of local sense amplifiers; and

b. a global sense amplifier, coupled with the plurality of local sense amplifiers, a selected one of the plurality of local sense amplifiers sensing the memory state and producing a local memory state signal representative thereof, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof, and wherein the plurality of memory cells coupled with the global sense amplifier is disposed as a memory column.

5. The memory module of Claim 3, wherein the plurality of memory cells comprises a memory cell subcolumn, and the local sense amplifier is coupled with a single memory cell subcolumn.

6. The memory module of Claim 3, wherein the plurality of memory cells is partitioned to form a plurality of memory cell subcolumns each having a respective plurality of memory cells, and the local sense amplifier is coupled with the plurality of memory cell subcolumns.

7. The memory module of Claim 4, further comprising a plurality of global sense amplifiers, selected ones of the plurality of global sense amplifiers having a respective plurality of local sense amplifiers coupled therewith, and selected ones of the plurality of local sense amplifiers being coupled with a respective plurality of memory cells, selected others of the plurality of global sense amplifiers being coupled with the selected ones such that the selected ones of the plurality of global sense amplifiers are local sense amplifiers relative to the selected others of the plurality of global sense amplifiers, each local sense amplifier producing a respective local memory state signal to which a corresponding global sense amplifier is responsive.

8. The memory module of Claim 1, wherein the local sense amplifier is responsive to a limited swing voltage signal from the memory cell representative of the memory state.

9. The memory module of Claim 2, wherein the global sense amplifier is responsive to a limited swing voltage signal representative of the memory state.

10. The memory module of Claim 8, wherein the global sense amplifier produces a limited swing voltage signal representative of the memory state.

11. The memory module of Claim 3, wherein one of the local sense amplifier is responsive to a limited swing voltage signal from the memory cell representative of the memory state.

12. The memory module of Claim 4, wherein one of the local memory state signal and the global memory state signal is a limited swing voltage signal.

13. The memory module of Claim 12, wherein both of the local memory state signal and the global memory state signal is a limited swing voltage signal.

14. The memory module of Claim 1, further comprising a local wordline decoder coupled with the memory cell, the local wordline decoder selecting the memory cell responsive to a local selection signal.

15. The memory module of Claim 2, further comprising a local wordline decoder coupled with the memory cell, the local wordline decoder selecting the memory cell responsive to a local selection signal.

16. The memory module of Claim 15, further comprising a global wordline decoder coupled with the local wordline decoder, the global wordline decoder producing the local selection signal responsive to a global selection signal.

17. The memory module of Claim 4, further comprising a plurality of local wordline decoders coupled with respective memory cells, a selected one of the plurality of local wordline decoders selecting one of the respective memory cells responsive to a local selection signal.

18. The memory module of Claim 17, further comprising a global wordline decoder coupled with the plurality of local wordline decoders, the global wordline decoder producing the local selection signal responsive to a global selection signal, and wherein the plurality of memory cells coupled with the global wordline decoder is disposed as a memory row.

19. The memory module of Claim 18, further comprising a plurality of global wordline decoders each coupled with a corresponding plurality of local wordline decoders, a selected one of the plurality of global wordline decoders producing a local selection signal responsive to a global selection signal.

20. The memory module of Claim 7, further comprising a plurality of local wordline decoders coupled with respective memory cells, selected ones of the plurality of local wordline decoders selecting respective memory cells responsive to a corresponding local selection signal.

21. The memory module of Claim 20, further comprising a global wordline decoder coupled with the plurality of local wordline decoders, the global wordline decoder producing the local selection signal responsive to a global selection signal, and wherein the plurality of memory cells coupled with the global wordline decoder is disposed as a memory row.

22. The memory module of Claim 21, further comprising a plurality of global wordline decoders, selected ones of the plurality of global wordline decoders being coupled with a respective plurality of local wordline decoders, selected ones of the plurality of local wordline decoders being coupled with a respective plurality of memory cells, selected others of the plurality of global wordline decoders

being coupled with the selected ones such that the selected ones are local wordline decoders relative to the selected others, each global wordline decoder producing a respective global selection signal to which the corresponding plurality of local wordline decoders is responsive.

23. The memory module of Claim 22, wherein one of the local memory state signal, the global memory state signal, the local selection signal, the global selection signal, and a combination thereof, comprises a limited swing voltage signal.

24. The memory module of Claim 22, wherein at least one of the global sense amplifier and the plurality of local sense amplifiers comprises one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

25. The memory module of Claim 22, further comprising a wordline decoder having a first memory row and a second memory row coupled therewith, the wordline decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

26. The memory module of Claim 22, further comprising:

a. a redundant memory row; and

b. a wordline decoder coupled an assigned memory row and the redundant memory row, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

27. The memory module of Claim 22, wherein one of the plurality of global wordline decoders and local wordline decoders comprises an asynchronously-resettable row decoder.

28. The memory module of Claim 27, wherein the asynchronously-resettable row decoder has a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

29. The memory module of Claim 22, having a designated group of memory cells assigned to represent a logical portion of the memory structure, the structure further comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

30. The memory module of Claim 29, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

31. The memory module of Claim 30, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

32. The memory module of Claim 31, wherein the plurality of selectable switches are fuses.

33. The memory module of Claim 31, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

34. The memory module of Claim 29, wherein each of the designated group and the redundant group comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

35. The memory module of Claim 25, wherein the wordline decoder includes a selection signal input, and further comprises comprises a multiplexer operably coupled with the first memory row and the second memory row, the multiplexer selectably directing the local selection signal from the wordline decoder selection signal input to the selected one of the first memory row and the second memory row.

36. The memory module of Claim 1, wherein the local sense amplifier comprises a high-precision delay measurement circuit.

37. The memory module of Claim 12, further comprising a high-precision delay measurement circuit constraining the limited voltage swing signal.

38. The memory module of Claim 37, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

39. The memory module of Claim 38, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation

signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

40. The memory module of Claim 39, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

41. The memory module of Claim 39, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

42. The memory module of Claim 41, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

43. The memory module of Claim 23, further comprising a high-precision delay measurement circuit constraining the limited voltage swing signal.

44. The memory module of Claim 43, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

45. The memory module of Claim 44, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

46. The memory module of Claim 45, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

47. The memory module of Claim 45, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

48. The memory module of Claim 47, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

49. The memory module of Claim 23, further comprising a diffusion replica delay circuit constraining the limited voltage swing signal.

50. The memory module of Claim 49, wherein the diffusion replica delay circuit comprises dummy cells operably coupled with a selected wordline decoder and a selected sense amplifier.

51. The memory module of Claim 50, wherein the dummy cells comprise split dummy bit lines.

52. The memory module of Claim 2, further comprising a data transfer bus circuit coupling the global sense amplifier to a data bus.

53. The memory module of Claim 52, wherein the data transfer bus circuit comprises a programmable driver, the programmable driver capable of imposing multilevel logic signals on the data bus.

54. The memory module of Claim 22, further comprising a data transfer bus circuit coupling a selected one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposing a limited voltage swing on the data bus.

55. The memory module of Claim 54, wherein the data transfer bus circuit comprises a programmable driver programmed to impose logic signals on the data bus.

56. The memory module of Claim 55, wherein the programmable driver is programmed to impose encoded signals on the data bus.

57. The memory module of Claim 55, wherein the programmable driver is programmed to impose multilevel logic signals on the data bus.

58. The memory module of Claim 22, wherein one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders comprises a limited swing voltage circuit, the limited swing voltage circuit producing a limited swing voltage signal of a respective one of the global memory state sign°al, the local memory state signal, the global selection signal, the local selection signal.

59. The memory module of Claim 1, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

60. The memory module of Claim 1, wherein the memory module is embedded in a communication device.

61. The memory module of Claim 22, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

62. The memory module of Claim 22, wherein the memory module is embedded in a communication device.

63. (Amended) The memory module of Claim 58, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

64. (Amended) The memory module of Claim 58, wherein the memory module is embedded in a communication device.

65. (Amended) A hierarchical memory structure, comprising:

a. memory cells having respective memory states;

b. local sense amplifiers selectively coupled with the memory cells, selected ones of the local sense amplifiers sensing the respective memory states and producing respective local memory state signals representative thereof, wherein the local sense amplifiers produce limited swing voltage signals;

c. local wordline decoders selectively coupled with the memory cells, selected ones of the local wordline decoders selecting respective memory cells responsive to a corresponding local selection signal;

A1

d. global sense amplifiers, selected ones of the global sense amplifiers being coupled with local sense amplifiers, selected ones of the local sense amplifiers being coupled with respective memory cells, selected others of the global sense amplifiers being coupled with the selected ones such that the selected ones of the global sense amplifiers are local sense amplifiers relative to the selected others of the global sense amplifiers in a multi-tiered hierarchy, each local sense amplifier producing a respective local memory state signal to which a corresponding global sense amplifier is responsive;

e. global wordline decoders, selected ones of the global wordline decoders being coupled with respective local wordline decoders, selected others of the global wordline decoders being coupled with the selected ones such that the selected ones are local wordline decoders relative to the selected others in a multi-tiered hierarchy, each global wordline decoder producing a respective global selection signal to which corresponding local wordline decoders are responsive;

f. one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier;

g. an asynchronously-resettable decoder;

h. a wordline decoder having a first memory row and a second memory row coupled therewith, the wordline decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal;

i. with the memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, a redundancy device, including:

(1) a redundant group of memory cells; and

(2) a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition,

wherein each of the designated group and the redundant group comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof;

A1

j. one of a diffusion replica delay circuit and a high-precision delay measurement circuit constraining a limited voltage swing signal; and

k. a data transfer bus circuit coupling a selected one of the global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposing a limited voltage swing on the data bus.

66. (Amended) The memory module of Claim 65, wherein the hierarchical memory structure is disposed in one of a semiconductor device, an optical device, and a combination thereof.

67. (Amended) The memory module of Claim 65, wherein the hierarchical memory structure is embedded in a communication device.

68. (Amended) A method for substantially simultaneously retrieving a first datum from a first memory location and storing a second datum in a second memory location, wherein both locations are disposed within a single-port hierarchical memory structure having local and global data sensing, and local and global location selecting, the method comprising:

A1

a. locally selecting the first memory location from which the first datum is to be retrieved;

b. locally sensing the first datum (READ operation);

c. globally selecting the second memory location;

d. substantially concurrently with the globally selecting, globally sensing the first datum at the first memory location;

e. outputting the first data subsequent to the globally sensing;

f. inputting the second datum substantially immediately subsequent to the outputting the first datum;

g. locally selecting the second memory location; and

h. storing the second datum (WRITE operation).

69. (Amended) The method of Claim 68, further comprising precharging bitlines coupled with the first and the second memory locations, prior to locally sensing the first datum (PRECHARGE operation).

70. (Amended) The method of Claim 68, wherein (a) through (h) are completed within one access cycle of the memory structure.

71. (Amended) The method of Claim 69, wherein a plurality of PRECHARGE-READ-WRITE operations are completed within one access cycle of the memory structure.

72. (Amended) A method for providing sequential storage of a first datum in a first hierarchical memory structure location and a second datum in a second hierarchical memory structure location within one access cycle of the memory structure, the structure having local and global location selecting, the method comprising:

A1

a. globally selecting the first hierarchical memory structure location to which the first datum is to be stored;

b. precharging bitlines coupled with the memory cells at the first hierarchical memory structure location (PRECHARGE1 operation);

c. locally selecting the first hierarchical memory structure location;

d. storing the first datum (WRITE1 operation);

e. globally selecting the second hierarchical memory structure location to which the second datum is to be stored;

f. substantially concurrently with the globally selecting the second hierarchical memory structure location, precharging bitlines coupled with the second hierarchical memory structure location (PRECHARGE2 operation);

g. locally selecting the second hierarchical memory structure location; and

h. storing the second datum (WRITE2 operation).

73. (Amended) A hierarchical memory structure comprising:

a. memory cells;

b. sense amplifiers coupled with the memory cells to form memory columns; and

c. decoders coupled with the memory cells to form memory rows,

wherein the memory cells, sense amplifiers, and decoders so coupled form a first tier memory module, and at least one of the first tier sense amplifiers and the first tier decoders provide a limited swing voltage signal.

74. (Amended) Thee hierarchical memory structure of Claim 73, further comprising:

A1

a. *(n-1)*-tier memory modules;

b. *(n)*-tier sense amplifiers coupled with the *(n-1)*-tier sense amplifiers in the *(n-1)*-tier memory modules; and

c. *(n)*-tier decoders coupled with the *(n-1)*-tier decoders in the *(n-1)*-tier memory modules,

wherein n > 1, and wherein the *(n-1)*-tier memory modules, *(n)*-tier sense amplifiers, and *(n)*-tier decoders so coupled form an *(n)*-tier memory module.

75. (Amended) The hierarchical memory structure of Claim 74, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders produces a limited swing voltage signal.

76. (Amended) The hierarchical memory structure of Claim 74, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

77. (Amended) The hierarchical memory structure of Claim 75, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

78. (Amended) The hierarchical memory structure of Claim 73, wherein one of plurality of first tier decoders is an asynchronously resettable row decoder.

79. (Amended) The hierarchical memory structure of Claim 73, further comprising one of a redundant memory row and a redundant memory column.

A1

80. (Amended) The hierarchical memory structure of Claim 74, wherein a selected one of the pluralities of *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

81. (Amended) The hierarchical memory structure of Claim 73, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

82. (Amended) The hierarchical memory structure of Claim 81, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

83. (Amended) The hierarchical memory structure of Claim 78, the asynchronously-resettable row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

84. (Amended) The hierarchical memory structure of Claim 75, wherein one of the *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

85. (Amended) The hierarchical memory structure of Claim 84, wherein a second selected one of the pluralities of *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

A1

86. (Amended) The hierarchical memory structure of Claim 84, wherein one of the decoders is an asynchronously resettable row decoder.

87. (Amended) The hierarchical memory structure of Claim 86, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

88. (Amended) The hierarchical memory structure of Claim 86, wherein the asynchronously-resettable row decoder is coupled with a first memory row and a second memory row, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

89. (Amended) The hierarchical memory structure of Claim 86, further comprising one of a redundant memory row and a redundant memory column.

90. (Amended) The hierarchical memory structure of Claim 89, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

91. (Amended) The hierarchical memory structure of Claim 74, having a designated group of memory cells assigned to represent a logical portion of the memory structure, the structure further comprising:

A1

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

92. (Amended) The hierarchical memory structure of Claim 91, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

93. (Amended) The hierarchical memory structure of Claim 92, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

94. (Amended) The hierarchical memory structure of Claim 93, wherein the plurality of selectable switches are fuses.

95. (Amended) The hierarchical memory structure of Claim 93, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

96. (Amended) The hierarchical memory structure of Claim 91, wherein each of the designated group and the redundant group comprise one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

97. (Amended) The hierarchical memory structure of Claim 75, further comprising a limited swing voltage driver circuit constraining the limited swing voltage signal.

A1

98. (Amended) The hierarchical memory structure of Claim 75, further comprising a high-precision delay measurement circuit constraining the limited swing voltage signal.

99. (Amended) The hierarchical memory structure of Claim 98, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

100. (Amended) The hierarchical memory structure of Claim 99, wherein the ring oscillator executes a plurality of oscillation cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

101. (Amended) The hierarchical memory structure of Claim 100, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

102. (Amended) The hierarchical memory structure of Claim 101, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

A1

103. (Amended) The hierarchical memory structure of Claim 102, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

104. (Amended) The hierarchical memory structure of Claim 75, further comprising a diffusion replica delay circuit constraining the limited voltage swing signal.

105. (Amended) The hierarchical memory structure of Claim 104, wherein the diffusion replica delay circuit comprises dummy cells operably coupled with a selected wordline decoder and a selected sense amplifier.

106. (Amended) The hierarchical memory structure of Claim 105, wherein the dummy cells comprise split dummy bit lines.

107. (Amended) The hierarchical memory structure of Claim 74, further comprising a data transfer bus circuit coupling a selected one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposed a limited voltage swing on the data bus.

A1

108. (Amended) The hierarchical memory structure of Claim 107, wherein the data transfer bus circuit comprises a programmable driver programmed to impose logic signals on the data bus.

109. (Amended) The hierarchical memory structure of Claim 108, wherein the programmable driver is programmed to impose encoded signals on the data bus.

110. (Amended) The hierarchical memory structure of Claim 108, wherein the programmable driver is programmed to impose multilevel logic signals on the data bus.

111. (NEW) In a hierarchical memory structure, a high-precision delay measurement circuit, comprising:

a. a ring oscillator having a plurality of oscillator stages, and executing oscillation cycles by circulating an oscillation signal therein, in response to an ENABLE signal, each of the oscillation cycle being executed in a predefined oscillation period;

A2

b. a controller coupled to the ring oscillator to selectively activate the ring oscillator with the ENABLE, and

c. oscillation signal detectors interposed between selected ones of the oscillator stages, selected ones of the oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

112. (NEW) The high-precision delay measurement circuit of Claim 114, further comprising a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

113. (NEW) The high-precision delay measurement circuit of Claim 112, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

A2

114. (NEW) The high-precision delay measurement circuit of Claim 112, wherein the oscillation counters comprise dual-edge detection counters.

115. (NEW) The high-precision delay measurement circuit of Claim 113, wherein the oscillation counters comprise dual-edge detection counters.

116. (NEW) The high-precision delay measurement circuit of Claim 111, further comprising a control signal output, the constraining a limited voltage swing signal.

117. (NEW) In a hierarchical memory structure, a decoder, comprising:

a. a synchronous portion, disposed to receive and responsive to a clocked signal;

b. an asynchronous portion, coupled with an asynchronous circuit; and

c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to a predetermined asynchronous reset signal.

118. (NEW) The decoder of Claim 117, wherein the feedback-resetting portion substantially isolates the synchronous portion from the asynchronous portion responsive to a predetermined monitor signal.

A2

119. (NEW) The decoder of Claim 117, further comprising an inverter and a plurality of buffer stages, selected ones of the plurality of buffer stages having a skew there between reducing load capacitance thereby.

120. (NEW) The decoder of Claim 117, wherein the decoder is an asynchronously-resettable row decoder.

121. (NEW) The decoder of Claim 117, wherein the decoder is an asynchronously-resettable column decoder.

122. (NEW) In a hierarchical memory structure, a decoder in a memory module having a plurality of memory cell groups, comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output,

wherein the decoder decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to an group-select signal.

123. (NEW) The decoder of Claim 122, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and a memory second memory cell, the multiplexer being responsive to the group-select signal.

A2

124. (NEW) The decoder of Claim 122, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

125. (NEW) The decoder of Claim 122, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein first memory column and a second memory column are adjacent memory column in the memory module, and the group-select signal is an alternative-column-select signal.

126. (NEW) The decoder of Claim 122, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-row-select signal.

127. (NEW) The decoder of Claim 122, wherein the decoder is a column decoder disposed in a memory module having assigned memory columns and a redundant memory column, and wherein the first memory row is an assigned memory column, the second memory column is the

redundant memory column and the group-select signal is a redundant-column-select signal.

128. (NEW) In a hierarchical memory structure, a decoder in a memory module having a plurality of memory cell groups, comprising:

a. a synchronous portion, disposed to receive and responsive to a clocked signal;

b. an asynchronous portion, coupled with an asynchronous circuit in a selected memory cell group;

c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to a predetermined asynchronous reset signal;

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d. a signal input;

e. a first memory output coupled with a first memory cell group;

f a second memory output coupled with a second memory cell group; and

g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to an group-select signal.

129. (NEW) The decoder of Claim 128, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and a memory second memory cell, the multiplexer being responsive to the group-select signal.

130. (NEW) The decoder of Claim 128, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

131. (NEW) The decoder of Claim 128, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein first memory column and a second memory column are adjacent memory column in the memory module, and the group-select signal is an alternative-column-select signal.

A2

132. (NEW) The decoder of Claim 128, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-row-select signal.

133. (NEW) The decoder of Claim 128, wherein the decoder is a column decoder disposed in a memory module having assigned memory columns and a redundant memory column, and wherein the first memory row is an assigned memory column, the second memory column is the redundant memory column and the group-select signal is a redundant-column-select signal.

134. (NEW) In a hierarchical memory structure having a memory component capacitance and memory component operational characteristics, a diffusion replica delay circuit, comprising:

a. a diffusion replica capacitor, coupled to the memory component, and capable of storing a predetermined replica charge representative of a selected memory component operational characteristic, and

b. a diffusion replica transistor, coupled with the diffusion replica capacitor, coupled between the diffusion replica capacitor and a charge sink, the transistor being disposed to control the magnitude of the predetermined replica charge.

135. (NEW) The diffusion replica delay circuit of Claim 134, wherein the memory component includes a dummy cell with a dummy bit line and a plurality of wordlines, the diffusion replica capacitor being coupled to the split dummy bit line and a limited number of wordlines.

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136. (NEW) The diffusion replica delay circuit of Claim 135, wherein the diffusion replica capacitor is coupled to one wordline.

137. (NEW) The diffusion replica delay circuit of Claim 134, wherein the memory component includes a plurality of access transistors having an access chain characteristic, and the diffusion replica transistor is disposed to be representative of the access chain characteristic.

138. (NEW) The diffusion replica delay circuit of Claim 135, wherein the memory component includes a plurality of access transistors having an access chain characteristic, and the diffusion replica transistor is disposed to be representative of the access chain characteristic.

139. (NEW) The diffusion replica delay circuit of Claim 136, wherein the selected memory component operational characteristic is a dummy bitline capacitance of a bitline coupled to the diffusion replica delay circuit, and the diffusion replica capacitance is substantially matched to the dummy bitline capacitance.

140. (NEW) The diffusion replica delay circuit of Claim 139, wherein the diffusion replica capacitance is substantially a predetermined fraction of the dummy bitline capacitance.

141. (NEW) The diffusion replica delay circuit of Claim 139, wherein the dummy cell is coupled with a memory cell having local bitlines and local wordlines, and the diffusion replica delay circuit provides a limited voltage swing signal to at least one of the local bitlines and the local wordlines.

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142. (NEW) The diffusion replica delay circuit of Claim 139, comprising dummy cells operably coupled with a selected wordline decoder and a selected sense amplifier.

143. (NEW) The diffusion replica delay circuit of Claim 142, wherein dummy cells are selectively coupled with memory cells, each having local bitlines and local wordlines, and the diffusion replica delay circuit provides a limited voltage swing signal to at least one of the local bitlines and the local wordlines.

144. (NEW) The diffusion replica delay circuit of Claim 143, wherein the dummy cells comprise split dummy bit lines.

145. (NEW) In a hierarchical memory structure, a limited swing driver, comprising:

a. a pass transistor coupled between a memory cell and an associated bitline;

b. an inverter having an input and an output, the output coupled to the gate of the pass transistor, selectively driving the pass transistor thereby, the inverter input being coupled with the memory cell, the coupling of inverter input and the memory cell forming a memory node; and

c. a discharge transistor coupled between the memory node and ground, the discharge transistor being driven by an input on the discharge transistor gate, the discharge transistor being programmed to produce a limited swing voltage at the memory node.

146. (NEW) The limited swing driver of Claim 145, wherein the limited swing voltage is less than about 350 mV.

147. (NEW) The limited swing driver of Claim 146, wherein the limited swing voltage is between about 300 mV and about 200 mV.

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148. (NEW) The limited swing voltage driver of Claim 145, further comprising at least one of:

a. a tri-state output enable isolating the memory node from the bitline, the bitline being one of a shared bitline and a multiplexed bitline; and

b. a self-reset circuit resetting the driver to a predetermined signal state.

149. (NEW) In a hierarchical memory structure, a sense amplifier, comprising:

a. a sampling circuit receiving an input signal to the sense amplifier;

b. a reference node storing a reference signal corresponding to the input data;

c. a timing circuit activating the sampling circuit for a predetermined interval, the sampling circuit admitting the reference signal to the reference node thereby.

150. (NEW) The sense amplifier of Claim 149, further comprising:

a. a pump capacitor substantially maintaining a value of the reference signal.

151. (NEW) The sense amplifier of Claim 149, further comprising:

a. a gain circuit coupled with the reference node and disposed to adaptively adjust gain of an output signal produced by the sense amplifier.

152. (NEW) The sense amplifier of Claim 149, wherein the sense amplifier is a single-ended sense amplifier.

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153. (NEW) In a hierarchical memory structure, a sense amplifier, comprising:

a. an amplifier offset cancellation network mitigating one of an inherent offset signal value and a dynamic offset signal value, and producing a residual offset signal value; and

b. an offset equalization network, substantially eliminating the residual offset signal value.

154. (NEW) The sense amplifier of Claim 153, wherein the amplifier offset cancellation network includes a plurality of precharge-and-balance pMOS transistors, and wherein the offset equalization network comprises at least one balancing pMOS transistor.

155. (NEW) The sense amplifier of Claim 153, wherein the sense amplifier is a differential sense amplifier.

156. (NEW) The sense amplifier of Claim 155, wherein the sense amplifier is a latch-type differential sense amplifier.

157. (NEW) The sense amplifier of Claim 154, wherein the sense amplifier is a latch-type differential sense amplifier.

158. (NEW) In a hierarchical memory structure, a sense amplifier adapted to sense corresponding global bitlines coupled thereto, comprising:

a. an isolation circuit, isolating the sense amplifier from the corresponding global bitlines when the sense amplifier is unused; and

b. a charge-sharing circuit, sharing charge between ones of the corresponding global bitlines, the charge-share circuit producing a limited voltage swing on the corresponding bit lines.

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159. (NEW) The sense amplifier of Claim 158, wherein the charge-sharing circuit comprises:

a. a precharging circuit, precharging ones of the corresponding bitlines, responsive to a bitline selection signal; and

b. a charge reservoir, selectively sourcing and sinking charge, being responsive when the sense amplifier is used.

160. (NEW) The sense amplifier of Claim 159, wherein the sense amplifier is a latch-type differential sense amplifier.

161. (NEW) In a hierarchical memory structure, a sense amplifier adapted to sense an input signal on corresponding global bitlines, comprising:

a. an amplifier offset cancellation network mitigating one of an inherent offset signal value and a dynamic offset signal value, and producing a residual offset signal value;

b. an offset equalization network, coupled with the amplifier offset cancellation network and substantially eliminating the residual offset signal value;

c. an isolation circuit, coupled between the sense amplifier and the corresponding global bitlines and isolating the

sense amplifier from the corresponding global bitlines when the sense amplifier is unused; and

d. a charge-sharing circuit, operably coupled with amplifier offset cancellation network, the offset equalization network, and the corresponding global bitlines, the charge-sharing circuit sharing charge between ones of the corresponding global bitlines, the charge-share circuit producing a limited voltage swing on the corresponding bit lines.

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162. (NEW) The sense amplifier of Claim 161, wherein the amplifier offset cancellation network includes a plurality of precharge-and-balance pMOS transistors, wherein the offset equalization network comprises at least one balancing pMOS transistor, wherein the charge-sharing circuit comprises a precharging circuit, precharging ones of the corresponding bitlines, responsive to a bitline selection signal; and a charge reservoir, selectively sourcing and sinking charge, being responsive when the sense amplifier is used.

163. (NEW) The sense amplifier of Claim 162, wherein the sense amplifier is a latch-type differential sense amplifier.

164. (NEW) In a hierarchical memory structure, a memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, the memory redundancy circuit, comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

165. (NEW) The memory redundancy circuit of Claim 164, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

166. (NEW) The memory redundancy circuit of Claim 165, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

A2

167. (NEW) The memory redundancy circuit of Claim 166, wherein the plurality of selectable switches are fuses.

168. (NEW) The memory redundancy circuit of Claim 167, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

169. (NEW) The memory redundancy circuit of Claim 164, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

170. (NEW) The memory redundancy circuit of Claim 164, further comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder

decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to an group-select signal.

171. (NEW) The memory redundancy circuit of Claim 170, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and a memory second memory cell, the multiplexer being responsive to the group-select signal.

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172. (NEW) The memory redundancy circuit of Claim 170, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

173. (NEW) The memory redundancy circuit of Claim 170, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein first memory column and a second memory column are adjacent memory column in the memory module, and the group-select signal is an alternative-column-select signal.

174. (NEW) The memory redundancy circuit of Claim 170, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-row-select signal.

175. (NEW) The memory redundancy circuit of Claim 170, wherein the decoder is a column decoder disposed in a memory module having assigned memory columns and a redundant memory column, and wherein the first memory row is an assigned memory column, the second memory column is the redundant memory column and the group-select signal is a redundant-column-select signal.

176. (NEW) In a hierarchical memory structure, a memory redundancy circuit in single-port hierarchical memory structure having a predetermined memory access speed and a memory access period, comprising:

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a. a memory module having

(1) memory cells disposed to store data, the memory cells including a designated group of memory cells being assigned to represent a logical portion of the memory structure and a redundant group of memory cells;

(2) hierarchically-coupled local and global sense amplifiers, the local sense amplifiers being coupled with the memory cells;

(3) hierarchically-coupled local and global row decoders, the local row decoders being coupled with the memory cells;

(4) a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition, and providing redundancy thereby;

b. hierarchically-coupled local and global sense amplifiers, selected local sense amplifiers being the global sense amplifiers of selected memory modules;

c. hierarchically-coupled local and global row decoders, selected local row decoders being the global row decoders of selected memory modules; and

d. a predecoding circuit coupled with selected global row decoders, wherein the predecoding circuit is disposed to provide predecoding at a speed substantially faster than the predetermined memory structure access speed, and allowing access to a selected memory cell at least twice during the memory access period, thereby providing dual-port functionality thereby.

177. (NEW) The memory redundancy circuit of Claim 176, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

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178. (NEW) The memory redundancy circuit of Claim 177, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

179. (NEW) The memory redundancy circuit of Claim 178, wherein the plurality of selectable switches are fuses.

180. (NEW) The memory redundancy circuit of Claim 179, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

181. (NEW) The memory redundancy circuit of Claim 176, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

182. (NEW) In a single-port hierarchical memory structure having local and global data sensing, local and global location selecting, and hierarchically-coupled memory modules having redundant groups of memory cells and a redundant memory location, wherein storage of a second datum at a designated memory location is to follow sensing of a first datum at the designated memory location, and wherein the designated memory location develops a "FAILED" condition, a method for substantially simultaneously retrieving a first datum from the designated memory location in the memory module and storing the second datum in the redundant memory location, the method comprising:

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a. locally selecting the designated memory location from which the first datum is to be retrieved;

b. locally sensing the first datum in the designated memory location (READ operation);

c. detecting the "FAILED" condition in the designated memory location;

d. assigning the redundant memory location to represent the designated memory location;

e. globally selecting the redundant memory location for storing the second datum;

f. substantially concurrently with the globally selecting, globally sensing the first datum in the designated memory location;

g. outputting the first datum subsequent to the globally sensing;

h. inputting the second datum substantially immediately subsequent to the outputting the first datum;

i. locally selecting the redundant memory location for storing the second datum; and

j. storing the second datum in the redundant memory location(WRITE operation).

183. (NEW) The method of Claim 182, further comprising precharging bitlines coupled with the memory location, prior to locally sensing the first datum (PRECHARGE operation).

184. (NEW) The method of Claim 183, wherein (a) through (j) (PRECHARGE-READ-WRITE operation) are completed within one access cycle of the memory structure.

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185. (NEW) The method of Claim 184, wherein a plurality of PRECHARGE-READ-WRITE operations are completed within one access cycle of the memory structure.

186. (NEW) In a hierarchical memory structure, a method for substantially simultaneously retrieving a first datum from a first memory location and storing a second datum in a second memory location, wherein both locations are disposed within a single-port hierarchical memory structure having local and global data sensing, and local and global location selecting, the method comprising:

a. locally selecting the first memory location from which the first datum is to be retrieved;

b. locally sensing the first datum (READ operation) in the first memory location;

c. globally selecting the second memory location;

d. substantially concurrently with the globally selecting, globally sensing the first datum at the first memory location;

e. outputting the first data subsequent to the globally sensing;

f. inputting the second datum substantially immediately subsequent to the outputting the first datum;

g. locally selecting the second memory location; and

h. storing the second datum (WRITE operation) in the second memory location.

187. (NEW) The method of Claim 186, further comprising precharging bitlines coupled with the first and the second memory locations, prior to locally sensing the first datum (PRECHARGE operation).

188. (NEW) The method of Claim 187, wherein (a) through (h) (PRECHARGE-READ-WRITE operation) are completed within one access cycle of the memory structure.

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189. (NEW) The method of Claim 188, wherein a plurality of PRECHARGE-READ-WRITE operations are completed within one access cycle of the memory structure.

190. (NEW) The method of Claim 186, wherein the first memory location is the same as the second memory location.

191. (NEW) In a hierarchical memory structure, a method for providing sequential storage of a first datum in a first hierarchical memory structure location and a second datum in a second hierarchical memory structure location within one access cycle of the memory structure, the structure having local and global location selecting, the method comprising:

a. globally selecting the first hierarchical memory structure location to which the first datum is to be stored;

b. precharging bitlines coupled with the memory cells at the first hierarchical memory structure location (PRECHARGE1 operation);

c. locally selecting the first hierarchical memory structure location;

d. storing the first datum (WRITE1 operation) in the first hierarchical memory structure location;

e. globally selecting the second hierarchical memory structure location to which the second datum is to be stored;

f. substantially concurrently with the globally selecting the second hierarchical memory structure location, precharging bitlines coupled with the second hierarchical memory structure location (PRECHARGE2 operation);

g. locally selecting the second hierarchical memory structure location; and

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h. storing the second datum (WRITE2 operation) in the second hierarchical memory structure location.

192. (NEW) The method of Claim 191, wherein (a) through (h) (WRITE-PRECHARGE-WRITE operation) are completed within one access cycle of the memory structure.

193. (NEW) The method of Claim 192, wherein a plurality of WRITE-PRECHARGE-WRITE operations are completed within one access cycle of the memory structure.

194. (NEW) The method of Claim 191, wherein the first hierarchical memory structure location is the same as the second hierarchical memory structure location.

195. (NEW) In a hierarchical memory structure, a single-port hierarchical memory structure having a predetermined memory access speed and a memory access period, comprising:

a. memory modules having

(1) memory cells disposed to store data;

(2) hierarchically-coupled local and global sense amplifiers, the local sense amplifiers being coupled with the memory cells; and

(3) hierarchically-coupled local and global row decoders, the local row decoders being coupled with the memory cells;

b. hierarchically-coupled local and global sense amplifiers, selected local sense amplifiers being the global sense amplifier of selected memory modules;

c. hierarchically-coupled local and global row decoders, selected local row decoders being the global row decoders of selected memory modules; and

d. a predecoding circuit coupled with selected global row decoders, wherein the predecoding circuit is disposed to provide predecoding at a speed substantially faster than the predetermined memory structure access speed, and allowing access to a selected memory cell at least twice during the memory access period, thereby providing dual-port functionality thereby.

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196. (NEW) The single-port hierarchical memory structure of Claim 195, wherein the predecoding circuit is disposed to provide predecoding at a speed more than twice the predetermined memory structure access speed, and allowing access to a selected memory cell three or more times during the memory access period, thereby providing multi-port functionality thereby.

197. (NEW) In a hierarchical memory structure, a memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, the memory redundancy circuit, comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

198. (NEW) The memory redundancy circuit of Claim 197, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

199. (NEW) The memory redundancy circuit of Claim 198, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

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200. (NEW) The memory redundancy circuit of Claim 199, wherein the plurality of selectable switches are fuses.

201. (NEW) The memory redundancy circuit of Claim 200, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

202. (NEW) The memory redundancy circuit of Claim 197, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

203. (NEW) The memory redundancy circuit of Claim 197, further comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder

decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to an group-select signal.

204. (NEW) The memory redundancy circuit of Claim 203, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and a memory second memory cell, the multiplexer being responsive to the group-select signal.

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205. (NEW) The memory redundancy circuit of Claim 203, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

206. (NEW) The memory redundancy circuit of Claim 203, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein first memory column and a second memory column are adjacent memory column in the memory module, and the group-select signal is an alternative-column-select signal.

207. (NEW) The memory redundancy circuit of Claim 203, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-row-select signal.

208. (NEW) The memory redundancy circuit of Claim 203, wherein the decoder is a column decoder disposed in a memory module having assigned memory columns and a redundant memory column, and wherein the first memory row is an assigned memory column, the second memory column is the redundant memory column and the group-select signal is a redundant-column-select signal.

209. (NEW) In a hierarchical memory structure, a controlled voltage swing data bus circuit for transferring data to a data bus, comprising:

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a. a pass transistor coupled with the bus;

b. a discharge transistor coupled with the pass transistor and ground, the discharge transistor programmed to impose a first preselected bus operational characteristic on the data bus; and

c. an inverter coupled between the discharge transistor and the pass transistor, the inverter and the discharge transistor forming a signal node, the inverter selectably driving the pass transistor gate, responsive to a signal node voltage value.

210. (NEW) The controlled voltage swing data bus circuit of Claim 209, wherein the pass transistor is programmed to impose a second preselected bus operational characteristic on the data bus.

211. (NEW) The controlled voltage swing data bus circuit of Claim 209, further comprising a plurality of discharge transistors, ones of the plurality of discharge transistors being selectively programmed to impose respective preselected bus operational characteristics on the data bus.

212. (NEW) The controlled voltage swing data bus circuit of Claim 209, wherein the pass transistor couples the data bus with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

213. (NEW) The controlled voltage swing data bus circuit of Claim 210, wherein the pass transistor couples the data bus with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

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214. (NEW) In a hierarchical memory structure, a controlled voltage swing data bus transfer circuit for transferring data between a first data bus and a second data bus, comprising:

a. a first inverter;

b. a first pass transistor, coupled between the first data bus and the first inverter, the coupling of the first pass transistor and the first inverter forming a first signal node;

c. a second inverter cross-linked to the first inverter;

d. a second pass transistor, coupled between the second data bus and the second inverter, the coupling of the second pass transistor and the second inverter forming a second signal node;

e. a first signal discharge transistor coupled between the first signal node and ground; and

f. a second signal discharge transistor coupled between the second signal node and ground, wherein the first inverter transfers a signal representative of first data on the first data bus to the second signal discharge transistor and the second inverter transfers a signal representative of second data on the second data bus to the first signal discharge transistor.

215. (NEW) The controlled voltage swing data bus transfer circuit of Claim 214, further comprising:

a. a first node charge transistor, coupled between V_{dd} and the first signal node;

b. a first node discharge transistor coupled between the first signal discharge transistor and ground;

c. a second charge transistor, coupled between V_{dd} and the second signal node;

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d. a second node discharge transistor coupled between the second signal discharge transistor and ground, wherein each of the first and second node charge transistors pull the respective first and second signal node to V_{dd}, when a LOW gate signal is applied thereto.

216. (NEW) The controlled voltage swing data bus transfer circuit of Claim 215, further comprising a clocking signal operably coupled with the first node charge transistor, the first node discharge transistor, the second node charge transistor, and the second node discharge transistor.

217. (NEW) The controlled voltage swing data bus transfer circuit of Claim 214, wherein one of the first data bus and the second data bus is coupled with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

218. (NEW) The controlled voltage swing data bus transfer circuit of Claim 216, wherein one of the first data bus and the second data bus is coupled with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.